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APPLICATION NO.	F	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,405	10/757,405 01/15/2004		Jun Takinosawa	MORI0006	4937
24203	7590	01/30/2006		EXAMINER	
GRIFFIN &	•	, PC	MARTINEZ, DAVID E		
SUITE PH-1 2300 NINTI	_	T. SOUTH	ART UNIT	PAPER NUMBER	
ARLINGTO			2181		
				DATE MAILED: 01/30/2000	5

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applic	ation No.	Applicant(s)					
Office Action Summary			7,405	TAKINOSAWA E	ET AL.				
			ner	Art Unit					
		David	E. Martinez	2182					
Period f	The MAILING DATE of this commun or Reply	ication appears on	the cover sheet with	the correspondence a	ddress				
WHI0 - Exte after - If NO - Failt Any	ORTENED STATUTORY PERIOD F CHEVER IS LONGER, FROM THE M nsions of time may be available under the provisions SIX (6) MONTHS from the mailing date of this comm o period for reply is specified above, the maximum stare to reply within the set or extended period for reply reply received by the Office later than three months a ed patent term adjustment. See 37 CFR 1.704(b).	IAILING DATE OF of 37 CFR 1.136(a). In n nunication. atutory period will apply ar will, by statute, cause the	THIS COMMUNICATE of event, however, may a reply and will expire SIX (6) MONTHS application to become ABANI	TION. be timely filed from the mailing date of this DONED (35 U.S.C. § 133).					
Status									
1)⊠	Responsive to communication(s) file	ed on <i>15 January 2</i>	2004.						
2a)□		2b)⊠ This action i							
3)□	Since this application is in condition	• "		, prosecution as to th	ne merits is				
•	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.								
Disposit	ion of Claims								
4)⊠	Claim(s) 1-20 is/are pending in the application.								
·	4a) Of the above claim(s) is/are withdrawn from consideration.								
5)□	Claim(s) is/are allowed.								
6)⊠	Claim(s) <u>1-20</u> is/are rejected.								
7)⊠	Claim(s) <u>1-20</u> is/are objected to.								
8)□	Claim(s) are subject to restrict	tion and/or electio	n requirement.						
Applicat	ion Papers								
9)[The specification is objected to by the	e Examiner.							
10)🖂	10)⊠ The drawing(s) filed on <u>15 January 2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.								
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).								
11)	The oath or declaration is objected to	by the Examiner.	Note the attached O	ffice Action or form P	'TO-152.				
Priority (under 35 U.S.C. § 119								
	12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).								
a)	a) All b) Some * c) None of:								
	1. Certified copies of the priority documents have been received.								
	2. Certified copies of the priority documents have been received in Application No								
	3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).								
* See the attached detailed Office action for a list of the certified copies not received.									
`	oo ino alaanaa astallaa omee astio		stance copies not rec	· ·					
Attachmen	• •		_						
1) Notic	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (P	TO 048)	4) Interview Sum	mary (PTO-413) ail Date					
3) 🛛 Infori	nation Disclosure Statement(s) (PTO-1449 or	PTO/SB/08)	5) Notice of Inform	all Date nal Patent Application (PT	'O-152)				
Paper No(s)/Mail Date <u>3/16/04</u> . 6) ☐ Other:									

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed 3/16/04 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Objections

Claims 1-20 are objected to because of the following informalities: Claims 1-20 fail to disclose what the "SDIO", "SD", "R/W FIFO", "RFIFO" and "WFIFO" acronyms stand for.

Applicant is advised to spell out what they stand for. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11, 16 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- 1. With regards to claims 11 and 20, line 4 of claim 11, and line 13 of claim 20 refer to the term "arbitrary write data". It is not clear what the term means. Write data can only be definite in a digital system and thus 'arbitrary write data' is indefinite.
- 2. With regards to claim 16, it is not understood if the SDIO controller is both talking to a host device only and then is also pluggable into a gps or a handyphone system or if in this case it is being connected to a gps or a handyphone instead of the host device, over the application interface and not through the use of the SD interface.

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Claim Rejections - 35 USC § 102

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The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10, 12-15 and 17-19, are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Application Publication No. US 2001/0006902 A1 to Ito.

- 3. With regards to claims 1, 12 and 17, Ito teaches an SDIO controller [fig 2 element 21] having a single-chip semiconductor device [fig 2 element 21] connecting a SDIO-compliant SDIO host device [paragraph 5, 83] with a plurality of applications via an SD bus, comprising:
 - (a) an SD interface [fig 2 element 21f] operably connectable with the SDIO host device [fig 2 element 10 operably connected to a host] to decode commands received from the SDIO host device, and to return a response to the SDIO host device [paragraphs 6, 38 and 44];
 - (b) one or more application interfaces [fig 2 element 21e]; and
 - (c) a temporary memory [fig 2 element 21d] operably connected between the SD interface [fig 2 element 21f] and the one or more application interfaces [fig 2 element 21e].
- 4. With regards to claim 2, Ito teaches an SDIO controller according to claim 1, wherein the temporary memory comprises an R/W FIFO device [fig 2 element 21d sram is a buffer that can be written into and read from paragraph 37].
- 5. With regards to claim 3, Ito teaches an SDIO controller according to claim 2, wherein the one or more application interfaces are selected from the group consisting of a PCMCIA

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interface, a PC card bus interface, a UART interface, and a memory interface [fig 2 element 21e].

- 6. With regards to claim 4, Ito teaches an SDIO controller according to claim 1, wherein the temporary memory [fig 2 element 21d] in the SDIO controller [fig 2 element 21] comprises as many read memories [fig 2 element 21d] as the number of application interfaces [fig 2 element 21e] to temporarily hold data read out of SDIO applications [sram is a work buffer memory paragraph 37]; and at least one write memory operably connected to temporarily hold data to be sent out to the SDIO host [sram is a work buffer memory paragraph 37].
- 7. With regards to claim 5, Ito teaches an SDIO controller according to claim 4, wherein each read memory is a RFIFO device [fig 2 element 21d sram is a buffer that can be read from paragraph 37] and the write memory is a WFIFO device [fig 2 element 21d sram is a buffer that can be written into paragraph 37].
- 8. With regards to claim 6, Ito teaches an SDIO controller according to claim 1, wherein the temporary memory in the SDIO controller comprises at least one read memory operably connected to temporarily hold data read out of SDIO applications [sram is a work buffer memory paragraph 37]; and at least one write memory operably connected to temporarily hold data to be sent out to the SDIO host [sram is a work buffer memory paragraph 37].
- 9. With regards to claim 7, Ito teaches an SDIO controller according to claim 6, wherein the read memory is a RFIFO device and the write memory is a WFIFO device [fig 2 element 21d sram is a buffer that can be written into and read from paragraph 37].
- 10. With regards to claim 8, Ito teaches an SDIO controller according to claim 2, further comprising a microcontroller unit [fig 2 element 21a] for data control, wherein the microcontroller unit is connected to control the SD interface [fig 2 element 21f] and the one or more application interfaces [fig 2 element 21e] [paragraphs 37 and 38].

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11. With regards to claim 9, Ito teaches an SDIO controller according to claim 8, further comprising an I/O device [fig 2 element 20 or element 21g] connected to input and output control signals to and from the microcontroller unit [fig 2 element 21a].

- 12. With regards to claim 10, Ito teaches an SDIO controller according to claim 9, wherein the I/O device is a general peripheral I/O device [fig 2 element 20 or element 21g].
- 13. With further regards to claims 12 and 17, Ito teaches an SDIO wireless communications card comprising:
- (b) a wireless communications module [fig 2 element 20] operably connected to the SDIO controller [fig 2 element 21] via the one or more application interfaces [fig 2 element 21f]; and
- (c) an SDIO-compliant card enclosure, wherein the SDIO controller and the wireless communications module are disposed within the enclosure [see figs 1A-1D which represent the outside of fig 2.].
- 14. With regards to claims 13 and 18, they are of the same scope as claim 2 above and thus are rejected under the same rationale.

With regards to claims 14 and 19, they are of the same scope as claim 8 above and thus are rejected under the same rationale.

With regards to claim 15, Ito teaches an SDIO wireless communications card according to claim 14, wherein the wireless communications module is selected from the group consisting of a IEEE 802.11b module, a IEEE 802.11a module, a IEEE 802.11g module, and a Bluetooth module [paragraph 33, 40].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. US 2001/0006902 A1 to Ito. In view of US Patent No. 6,748,482 to Fackenthal.

15. With regards to claim 11, Ito teaches an SDIO controller according to claim 10, wherein the microcontroller unit operates to decode data when the data sent from the SDIO host device to the SDIO controller via the SD bus [see paragraphs 6, 38 and 44] contains at least a register read/write address [done in a write or read operation], a selected type of operation [done in a write or read operation], a quantity of data [done in a write or read operation], and arbitrary write data [done in a write or read operation. Ito fails to explicitly disclose the microcontroller unit operates to access non-contiguous registers via an application interface. However, Fackenthal teaches it is common for an application interface to access data in flash memory from contiguous and non-contiguous registers for the benefit archiving data into available memory even if it's scattered, and then being able to retrieve it at a later time [column 1 lines 24-42].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Ito and Fackenthal to have the microcontroller unit operates to access non-contiguous registers via an application interface for the benefit archiving data into available memory even if it's scattered, and then being able to retrieve it at a later time.

16. With regards to claim 20, it is of the same scope as the combination of claims 1, 11 and 12, and thus is rejected under the same rationale.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. US 2001/0006902 A1 to Ito. In view of US Patent Application Publication No. US 2004/0225796 A1 to Hanson et al. (hereinafter Hanson).

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17. With regards to claim 16, Ito fails to teach an SDIO wireless communications card according to claim 15, further comprising one or more additional applications selected from the group consisting of a global positioning system and a personal handyphone system, wherein the one or more additional applications are operably connected to corresponding application interfaces of the SDIO controller. However, Hanson teaches an SD integrated memory card having a global positioning system operably connected to an application interface within the SD card for the benefit of providing GPS services to a user [paragraph 17].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Ito and Chang to have the SDIO wireless communication card comprise a global positioning system (GPS) application operably connected to an application interface within the SDIO card for the benefit of providing GPS services to a user.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MARAPETTON AMINER